From June 2010 *High Frequency Electronics*

Design Method for the Fastest Settling Type 2 Phase Lock Loop: Part 1

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The author shows that mapping the denominator of the closed loop PLL transfer function to the Gaussian function results in the fastest settling time

Fast settling time is always desirable in any PLL (phase lock loop), as long as the noise performance is within limit. One application where fast settling is of high importance is in the design of a network analyzer. A PLL is used to synthesize both the source signal for the device under test and the LO signal for down conversion. With a faster settling source and LO, more measurements can be done for a given period of time, thus improving measurement throughput. In a test environment, this improvement directly yields higher productivity, since more parts can be tested. In addition to that, faster sweep time in a network analyzer will enable a user to approach real time measurement to capture any intermittent signal or glitches.

Settling time in this case refers to the time it takes for the loop to pull the frequency error F_{err} at the phase frequency detector output ($F_{vco}N - F_{ref}$ as in Figure 1) to the specified frequency, without the PLL losing lock. This process is linear so the settling can be conveniently analyzed through the use of a transfer function. If the initial F_{err} is larger than the pull out range of the PLL, the loop will lose lock or "cycle slip" and acquisition will need to take place before settling can take place. This paper only discusses settling, assuming that is the F_{err} is always less than the pull out range and the loop never loses lock.

When it is required to change the output frequency of a PLL, the first thing that needs to happen is to either change the divider value N at the feedback path or change the reference frequency F_{ref}. The former is usually the case. The changes of N will be in a step and as the loop never lose lock, the settling time can be analyzed. The basic procedure is to calculate the close loop transfer function and multiply it with the step input. Through inverse Laplace transform, the output response in time domain can be analyzed and the settling time can be quantified.

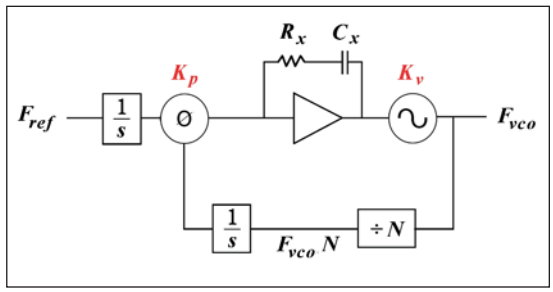

Figure 1 · Type 2 PLL block diagram.

Most of the time, the settling time is analyzed by looking at the F_{err} but in this paper, the settling time is analyzed through F_{vco} since this is the variable that we want to have the fastest settling. The F_{vco} could have settled while the F_{err} is still trying to find a stable point, or vice versa.

Usually, the closed loop transfer function is defined as the ratio of $\theta_{vco}/\theta_{ref}$ where θ_{vco} and θ_{ref} are the phase of the VCO and the Reference signal, respectively. As we are interested in analyzing the settling of the frequency rather than the phase, the ratio needs to be changed to F_{vco}/F_{ref}. Figure 1 shows the PLL block diagram whereby the input and the output are in frequency, rather than in phase. As far as close loop transfer function, $\theta_{vco}/\theta_{ref}$ will be the same as F_{vco}/F_{ref} as shown in (1).

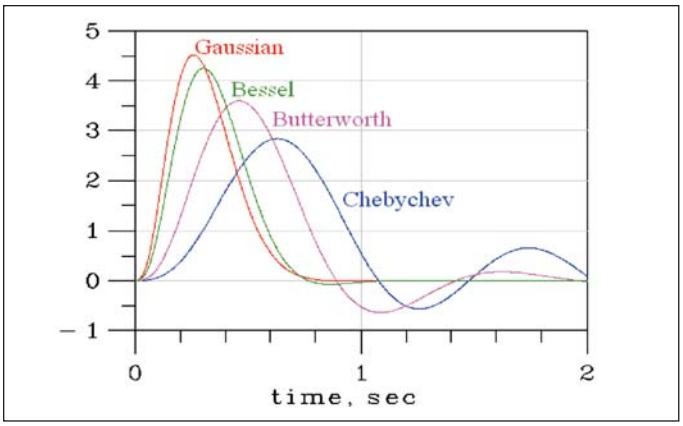

Figure 2 · Settling time of different LPFs, driven with an impulse input.

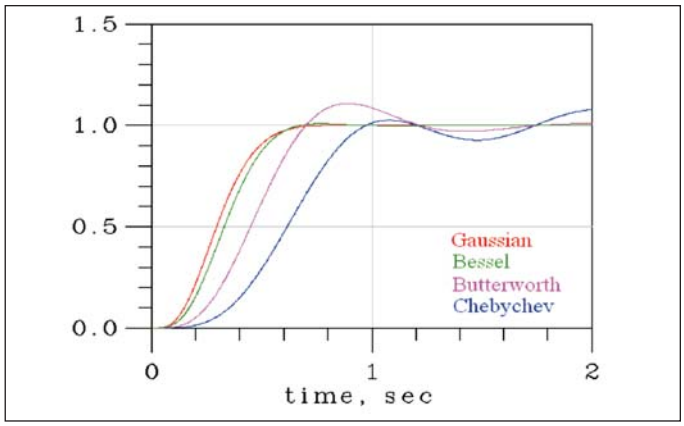

Figure 3 · Settling time of different LPF, driven with step input.

$$\frac{\theta_{vco}}{\theta_{ref}} = \frac{(F_{vco}/s)}{(F_{ref}/s)} = \frac{F_{vco}}{F_{ref}} \tag{1}$$

Figure 1 is a generic 2nd order Type 2 charge pump PLL that consist of charge pump phase detector, loop filter, VCO and Divider on the feedback path. Even though *charge pump PLL* is used throughout the analysis, the final results achieved can be adapted to another PLL whereby the output of the phase detector is a voltage rather current. The abbreviation *PLL* will be used throughout the analysis for simplicity. The R_z and C_z on the loop filter create the zero required for Type 2 PLL stability. K_p and K_v (highlighted in red) are the gain of the phase detector and the VCO respectively.

Research and design work related to fast settling PLL are not many and this paper will cover that in detail. The approach presented here is to achieve the fastest settling Type 2 PLL, by taking the advantage of Gaussian function which, from linear control theory, is well known to provide the fastest rise time and fall time, with no overshoot, in response to a step function input. Not only does a Gaussian function provide the fastest settling for a step input, but it also provides the fastest settling to an impulse input.

Theory and Discussion

As the closed loop transfer function F_{vco}/F_{ref} is that of a low pass filter (LPF), several LPFs of different topologies were synthesized using ADS and the settling response in the time domain to a step input and impulse input were analyzed. The 3 dB cutoff of all the filters were normalized to 1 rad/s and the order is set to 4. This is to graphically prove that a Gaussian filter does provide the fastest settling, compared to other filter topologies. Figure 2 is the impulse response of the LPFs. Even though Gaussian has the highest overshoot, it is actually the fastest to settle; well within 1 second. Figure 3 is the step response and Gaussian LPF has the fastest rise time and peaks with a little bit of overshoot, if we zoom in very close.

A true Gaussian filter should not have any overshoot at all on the step response. The reason for the small overshoot on the step response is due to the polynomial equations used to approximate Gaussian magnitude function which is defined in (2).

$$|H(s)| = e^{s^2} \tag{2}$$

A series with an infinite number of terms is required in order to truly represent the Gaussian response of (2). A polynomial approximation is typically used to make the filter realizable through resistor R, inductor L and capacitors C. This filter is called polynomial filters. For a 3rd order approximation, (2) can be approximated by (3)

$$H(s) = \frac{a_0}{s^3 + a_2 s^2 + a_1 s + a_0} \tag{3}$$

where a_2, a_1 and a_0 are the coefficients of the polynomial, and it determines the topology of the filters, whether Gaussian, Butterworth, Bessel and so on.

Achieving exactly Gaussian response where there is no overshoot on the step response, is not entirely possible in a Type 2 PLL since a zero in the numerator of the closed loop transfer function will give rise to an overshoot, when driven with step input. A true Gaussian function, approximated through polynomials as in (3), only has poles but not zeros. The zero in a Type 2 PLL is required for the loop stability since typically, n–1 zero is required for a type n loop.

In a circumstance where a true Gaussian response is desired, Type 1 PLL can be used where there will be no zero in the numerator of the close loop transfer function. Removing the zero in the numerator of the PLL closed loop transfer function eliminates the impulse output

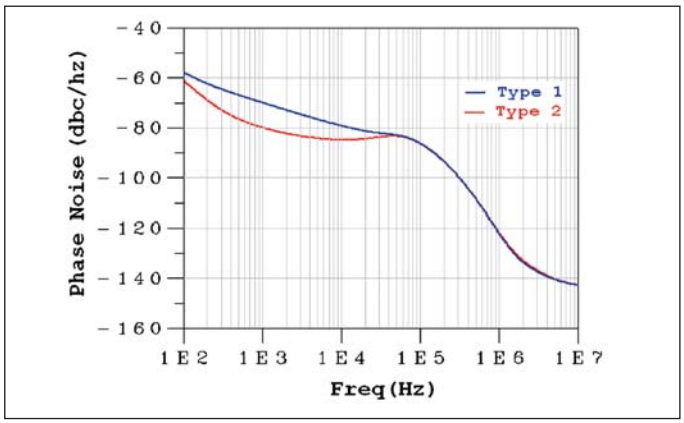

Figure 4 · Typical phase noise of a PLL, comparing Type 1 and Type 2.

which may look like an overshoot, so fastest settling time can be achieved. Extensive considerations need to be taken when choosing Type 1 PLL since in many aspects, Type 2 is far more superior. The next two paragraphs explain the downsides of a Type 1 PLL.

The DC gain in Type 2 is limited only by the open loop gain of the op amp used for the loop filter. This large DC gain in Type 2 will force the static phase error at the phase detector output to be close to zero, or it can be set constant at one value. The static phase error in a Type 1 PLL is not constant, but depends on VCO output frequency. The phase error will be such that a correct tuning voltage is generated to produce required output at the VCO. This difference is significant since we typically want to operate the phase detector close to 0º phase error to minimize reference energy feed through and at the same time ensure that the phase detector is operating in the most linear region. Since the phase error in Type 1 varies, at some output frequencies, the phase detector could be forced to operate at its "dead zone," where intermittent unlock could take place and phase noise degradation could be a problem.

Another benefit of a Type 2 PLL is that the VCO's phase noise inside the LBW will be attenuated at 40 dB/decade whereas in Type 1, the attenuation is only 20 dB/dec. Figure 4 shows the comparison between type 1 and type 2 PLL phase noise. The LBW is roughly around 80 kHz. For a microwave VCO that works up to 10 GHz, a GaAs FET is typically used as the active device to generate the negative resistance. GaAs FETs have a high 1/*f* corner frequency of few MHz, and this will cause the VCO's phase noise to have 30 dB/dec roll off, up to that 1/*f* corner frequency. So, if type 1 PLL is used together with a microwave GaAs FET VCO, within the LBW, the phase noise contribution of the GaAs VCO at the PLL output would have a slope of 30 dB/dec – 20 dB/dec = 10 dB/dec. This is apparent in Figure 4 where the Type 1 phase noise rolls off from 60 dBc/Hz at 100 Hz offset, to 80 dBc/Hz at 10 kHz offset. Based on these two reasons, the Type 1 PLL is rarely used.

So how do we design a type 2 PLL that takes advantage of Gaussian fast settling performance? Recall that the PLL close loop response is lowpass and with a zero on the numerator, whereas Gaussian function has no zero on the numerator. Trying to match the two curves or trying to match the two transfer functions will not work, mainly due to the zero that PLL closed loop transfer function has. We start by defining the closed loop transfer function of the PLL as shown in (4). Without loss of generality, a 3rd order loop is used.

$$\frac{F_{vco}}{F_{ref}}(s) = \frac{K_2(s+\omega_z)}{s^3 + a_2 s^2 + a_1 s + a_0} \tag{4}$$

In (4), K_2 is just a constant and ω_z is the zero to make the loop of Type 2. a_2, a_1 and a_0 are the coefficients of the denominator, as in (3). To understand the settling of F_{vco}, we multiply (4) with $\Delta F_{ref}/s$, as shown in (5).

$$F_{vco}(s) = \frac{\Delta F_{ref}}{s} \frac{K_2(s+\omega_z)}{s^3 + a_2 s^2 + a_1 s + a_0} \tag{5}$$

F_{ref} is the step change at the reference port which will cause F_{vco} to change. As discussed at the beginning of this paper, when we want to change F_{vco}, we usually accomplish this by changing the divider N. Let say the current VCO frequency is F_{vco} and the current divider N is N_{old}. When N_{old} is changed to N_{new}, the corresponding step at the reference port is shown in (6). This value can then be substituted into (5)

$$\Delta F_{ref} = \left(\frac{N_{old}}{N_{new}} - 1\right) F_{ref} \tag{6}$$

Expanding and simplifying (5), we can rewrite it as:

$$F_{vco}(s) = \left(K_3 + \frac{K_4}{s}\right) \frac{a_0}{s^3 + a_2 s^2 + a_1 s + a_0} \tag{7}$$

K_3 and K_4 are just constants. By analyzing (7), we can say that the *step response of a Type 2 PLL is equivalent to the sum of the step response and impulse response of a low pass filter* whose transfer function is defined in (3). K_3 is the impulse input and K_4/s is the step input.

Understanding (7) is the key to designing the fastest settling PLL. As graphically shown in Figures 2 and 3, Gaussian LPF provides the fastest settling when excited with either impulse input or step input. So if the denominator of the PLL transfer function is mapped to the Gaussian LPF denominator, that is a_2, a_1 and a_0 are selected so that it approximates a Gaussian function, then a

n	C_{1N}	L_{2N}	C_{3N}	L_{4N}	C_{5N}	L_{6N}	C_{7N}
2	1.3294	0.3894					
3	1.4179	0.7167	0.2347				
4	1.4518	0.8406	0.4905	0.1642			
5	1.4655	0.8934	0.6109	0.3684	0.1239		
6	1.4713	0.9174	0.6710	0.4792	0.2915	0.0981	
7	1.4737	0.9286	0.7020	0.5412	0.3918	0.2387	0.0803

Table 1 · Gaussian low pass filter components, where the value is normalized to ω_{3dB} =1 rad/s and R_s = 1.

Type 2 PLL with the fastest settling time can be achieved.

It might look easy to just solve for a_2, a_1 and a_0 but as will be shown, they depend on several variables—for example, the loop gain, ω_z, the pole ω_p and few others. On top of that, the LBW required is not the $f_{3\,dB}$ of the Gaussian filter thus making it more complicated. Instead of solving for a_2, a_1 and a_0, the set of variables that make a_2, a_1 and a_0 will be solved. 2nd Order Type 2 up to 7th Order Type 2, will be analyzed.

2nd Order Type 2 Fastest Settling PLL

2nd Order Type 2 PLL should have a closed loop transfer function as defined in (8). The objective is to map the 2nd order denominator in (8), to the 2nd order Gaussian LPF. We start by coming up with a normalized L and C for the LPF. To simplify the analysis, the singly terminated topology where the load impedance is infinite is used.

$$L_n = \frac{L_{nN}}{\omega_{3db}} \tag{8}$$

Table 1 lists the normalized values of L_{nN} and C_{nN} for 2nd, 3rd, 4th, 5th, 6th and 7th order Gaussian filter, where the ω_{3dB} is normalized to 1 rad/s. Figure 5 is the equivalent circuit for the nth order and singly terminated filter, that will be used together with the normalized L_{nN} and C_{nN} listed in Table 1. In Figure 5, for even order, C_n should be deleted, and L_n should be the first component after the 1 ohm.

The source resistance is normalized to 1 ohm and the load is infinite, hence singly terminated. The normalized components L_{nN} and C_{nN} need to be scaled for a different ω_{3dB} cutoff, as per (9) and (10). There is no source impedance to be defined for a PLL so it is left at 1 ohm, which is going to simplify the analysis.

$$L_n = \frac{L_{nN}}{\omega_{3db}} \tag{9}$$

$$C_n = \frac{C_{nN}}{\omega_{3db}} \tag{10}$$

For 2nd order filter, the equivalent circuit is shown in Figure 6 and the transfer function is shown in (11)

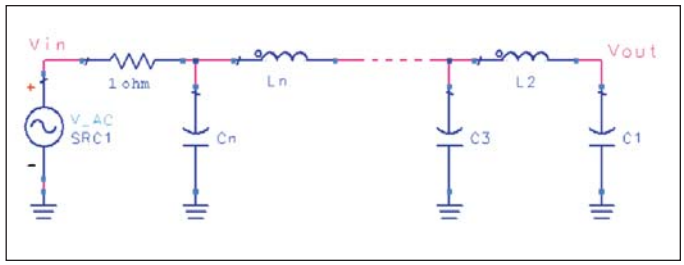

Figure 5 · Generic circuit to be used for the Gaussian low pass filter.

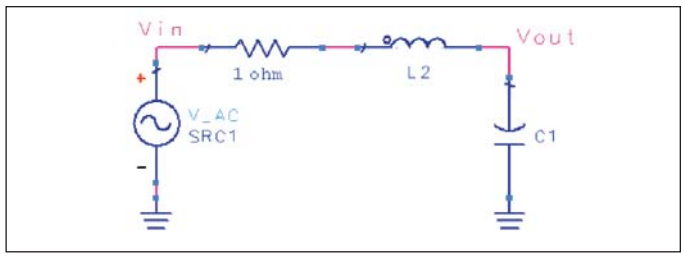

Figure 6 · 2nd order low pass filter circuit.

$$H(s) = \frac{1}{L_2 C_1} \frac{1}{s^2 + \frac{s}{L_2} + \frac{1}{L_2 C_1}} \tag{11}$$

We can now proceed to calculate the closed loop transfer function of the PLL. The circuit shown in Figure 1 is actually of 2nd order Type 2 PLL so we can use this figure to calculate the transfer functions. The open loop gain $OL(s)$ is shown in (12) and is calculated by multiplying the gain around the loop.

$$OL(s) = \frac{K_p}{sC_z}\left(1 + \frac{s}{\omega_z}\right)\frac{K_v}{Ns} \tag{12}$$

The LBW can be calculated from (12) by setting the OL gain to 1 and $s = j\omega_0$, where ω_0 is the unity crossover frequency or the LBW. From this point onward, ω_0 will be used to represent LBW. This is shown in (13).

$$1 = \frac{K_p}{\omega_0^2 C_z}\sqrt{1 + \frac{\omega_0^2}{\omega_z^2}}\frac{K_v}{N} \tag{13}$$

The ω_0 can be solved after rearranging (13), as shown in (14). X_{oz} is the ratio of ω_0 to ω_z, as in (14), and the value is a constant that needs to be solved in order for the denominator of the close loop transfer function to be of Gaussian. By knowing X_{oz}, we will have knowledge on where to place ω_z, based on the required ω_0.

$$\omega_0^2 = \frac{K_p}{C_z}\sqrt{1 + X_{oz}^2}\frac{K_v}{N} \tag{14}$$

$$X_{oz} = \frac{\omega_o}{\omega_z} \tag{15}$$

The closed loop transfer function $CL(s)$ can be calculated using the famous negative feedback equation defined in (16), where $A(s)$ is the forward gain and $B(S)$ is the feedback gain. $1/s$ is the frequency to phase converter at the input of the PFD.

$$CL(s) = \frac{1}{s}\frac{A(s)}{1 + A(s)B(s)} \tag{16}$$

Based on this, the close loop transfer function $CL(s)$ can be shown to be of (17),

$$CL(s) = \frac{1}{\omega_z C_z}\frac{K_p K_v(\omega_z + s)}{s^2 + \frac{K_p K_v}{N\omega_z C_z}s + \frac{K_p K_v}{NC_z}} \tag{17}$$

Substituting (14) and (15) into (17), we arrive at (18).

$$CL(s) = \frac{1}{\omega_z C_z}\frac{K_p K_v(\omega_z + s)}{s^2 + \frac{\omega_o X_{oz}}{\sqrt{1 + X_{oz}^2}}s + \frac{\omega_o^2}{\sqrt{1 + X_{oz}^2}}} \tag{18}$$

Now we can equate the denominator of (18) to the denominator of (11). The two equalities are shown in (19) and (20)

$$\frac{\omega_o X_{oz}}{\sqrt{1 + X_{oz}^2}} = \frac{1}{L_2} \tag{19}$$

$$\frac{\omega_o^2}{\sqrt{1 + X_{oz}^2}} = \frac{1}{L_2 C_1} \tag{20}$$

What we want to find are the constants X_{oz}, ω_0, and ω_{3dB}. The equivalent ω_{3dB} for the low pass filter does not equal to ω_0 but the ratio of the two will be a constant, just like X_{oz}. A new variable call X_{of} is defined in (21)

$$X_{of} = \frac{\omega_o}{\omega_{3db}} \tag{21}$$

Substituting (9) and (10) into (19) and (20), and using (21), we arrive at (22) and (23)

$$\frac{X_{of} X_{oz}}{\sqrt{1 + X_{oz}^2}} = \frac{1}{L_{2N}} \tag{22}$$

$$\frac{X_{of}^2}{\sqrt{1 + X_{oz}^2}} = \frac{1}{L_{2N} C_{1N}} \tag{23}$$

Solving (22) and (23) simultaneously, the value of X_{oz} and X_{of} can be calculated.

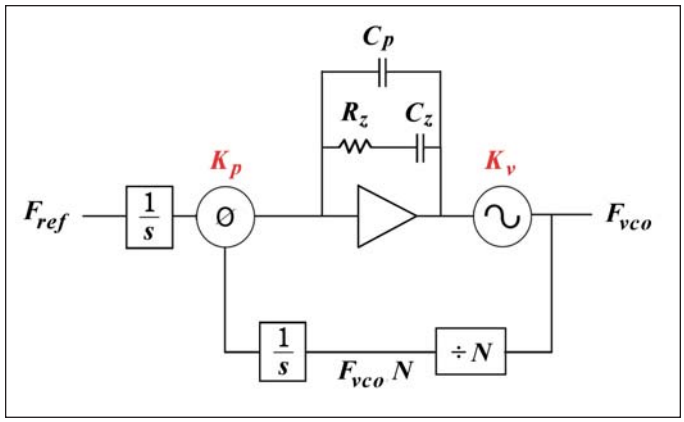

Figure 7 · 3rd order Type 2 PLL.

$$X_{oz} = 3.5476 \tag{24}$$

$$X_{of} = 2.6735 \tag{25}$$

For example, let say a fastest settling 2nd order Type 2 PLL with $\omega_0 = 100$ krad/s need to be designed. First thing to do is to calculate ω_z which is simply $\omega_z = \omega_0/X_{oz} = 28.19$ krad/s. Usually R_z shown in Figure 1 is set first so that a small value can be chosen. A small R_z value is favorable for lower noise. The value of C_z can be calculated accordingly. Once C_z is calculated, then the value of K_p required to set the ω_0 =100 krad/s can be calculated. Solving K_p in (13), we achieve (26). (26) assumes that K_p can be varied so that the ω_0 can be set accordingly.

$$K_p = \frac{\omega_0^2 C_z N}{\sqrt{1 + X_{oz}^2} K_v} \tag{26}$$

X_{of} is not being used as far as PLL design is concerned, but will be used to indicate the settling speed of the PLL. For this example, ω_{3dB} is lower than ω_0 by a factor of 2.6735. The absolute value ω_{3dB} is 37.4 krad/s. So even though the LBW is designed at ω_0 =100 krad/s, the equivalence ω_{3dB} of the Gaussian LPF is 37.4 krad/s. That means the PLL will have a settling speed of 37.4 krad/s Gaussian LPF.

As far as settling speed is concerned, the smaller the value of X_{of} the faster is the settling time of the PLL. It will be shown empirically that the higher the order of the PLL, the smaller is the value of X_{of}, which means that a higher order loop is faster, for a given ω_0.

At this point, the stability of the PLL needs to be verified as well and this can be done through the phase margin. The phase margin is the sum of $OL(s)$ phase and 180°, at ω_0. From (12), the phase margin can be calculated as follows,

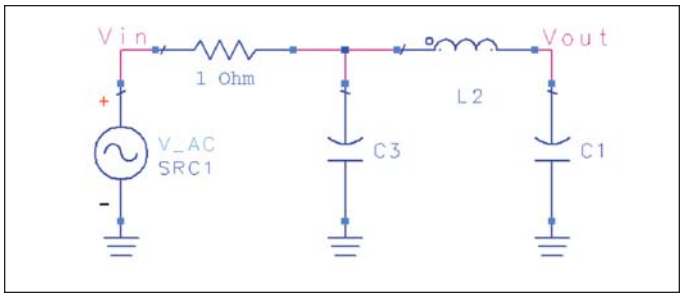

Figure 8 · 3rd order low pass filter circuit.

$$PM = -90^o + phase(1 + j\frac{\omega_o}{\omega_z}) - 90^o + 180^o$$

$$PM = 74.258°$$

With a phase margin of 74.258, the stability of the PLL is guaranteed.

3rd Order Type 2 Fastest Settling PLL

A 3rd order type 2 PLL will have additional capacitor C_p as shown in Figure 7. A 3rd order PLL will have a higher rejection of F_{ref}, so any feed through or "junk" from F_{ref} will be further attenuated. The treatment of a 3rd order PLL is similar to 2nd order, but of course with higher complexity.

We start with the 3rd order Gaussian LPF, which has the normalized values listed in Table 1. Figure 8 shows the corresponding schematic.

The transfer function of the circuit in Figure 8 can be shown to be of (27).

$$H(s) = \frac{1}{C_3 L_2 C_1} \frac{1}{s^3 + \frac{s^2}{C_3} + (\frac{1}{L_2 C_1} + \frac{1}{L_2 C_3})s + \frac{1}{L_2 C_3 C_1}} \tag{27}$$

We can now proceed to calculate the $OL(s)$ of the PLL in Figure 7. The R_z, C_z and C_p will create a zero ω_z and a pole ω_p as defined in (28) and (29)

$$\omega_z = \frac{1}{R_z C_z} \tag{28}$$

$$\omega_p = \frac{1}{R_z \frac{C_z C_p}{C_z + C_p}} \tag{29}$$

The $OL(s)$ of the PLL, substituting (28) and (29), is shown in (30).

$$OL(s) = K_p \frac{(1 + \frac{s}{\omega_z})}{s(1 + \frac{s}{\omega_p})(C_z + C_p)} \frac{K_v}{Ns} \tag{30}$$

The ω_0 can be calculated from (30) by setting the OL gain to 1 and set s = jω_0. This is shown in (31). X_{oz} is the ratio of ω_0 to ω_z, as in (15), and X_{op} is the ratio of ω_p to ω_p, defined in (32). These two values are constants that need to be solved in order for the denominator of the close loop transfer function to be of Gaussian. By knowing X_{oz} and X_{op}, we will have a knowledge on where to place ω_z and ω_p, based on the required ω_0.

$$\omega_0^{\,2} = \frac{K_p K_v \sqrt{1+X_{oz}^{\,2}}}{N(C_z+C_p)\sqrt{1+X_{op}^{\,2}}} \tag{31}$$

$$X_{op} = \frac{\omega_o}{\omega_p} \tag{32}$$

Based on (16), the $CL(s)$ is calculated and the final result is shown in (33), after substituting (34) in. M_3 is just a constant to simplify $CL(s)$.

$$CL(s) = \frac{K_p K_v(\omega_z+s)}{\omega_z(C_z+C_p)} \frac{\omega_p}{s^3 + \frac{\omega_o}{X_{op}} s^2 + \omega_o^{\,2} X_{oz} M_3 s + \omega_o^{\,3} M_3} \tag{33}$$

$$M_3 = \frac{\sqrt{1+X_{op}^{\,2}}}{X_{op}\sqrt{1+X_{oz}^{\,2}}} \tag{34}$$

Now we can equate the denominator of (33) to the denominator of (27).

$$\frac{\omega_o}{X_{op}} = \frac{1}{C_3} \tag{35}$$

$$\frac{\omega_o^{\,2} X_{oz}}{X_{op}} \frac{\sqrt{1+X_{op}^{\,2}}}{\sqrt{1+X_{oz}^{\,2}}} = \frac{1}{L_2 C_1} + \frac{1}{L_2 C_3} \tag{36}$$

$$\frac{\omega_o^{\,3}}{X_{op}} \frac{\sqrt{1+X_{op}^{\,2}}}{\sqrt{1+X_{oz}^{\,2}}} = \frac{1}{L_2 C_3 C_1} \tag{37}$$

Again, instead of solving for ω_0, we would like to solve for X_{of} defined in (21). (35)-(37) can be rewritten as follow,

$$\frac{X_{of}}{X_{op}} = \frac{1}{C_{3N}} \tag{38}$$

$$\frac{X_{of}^{\,2} X_{oz}}{X_{op}} \frac{\sqrt{1+X_{op}^{\,2}}}{\sqrt{1+X_{oz}^{\,2}}} = \frac{1}{L_{2N} C_{1N}} + \frac{1}{L_{2N} C_{3N}} \tag{39}$$

$$\frac{X_{of}^{\,3}}{X_{op}} \frac{\sqrt{1+X_{op}^{\,2}}}{\sqrt{1+X_{oz}^{\,2}}} = \frac{1}{L_{2N} C_{3N} C_{1N}} \tag{40}$$

Solving (38) to (40) simultaneously, the value of X_{op}, X_{oz} and X_{of} can be calculated.

$$X_{oz} = 2.6811 \tag{41}$$

$$X_{op} = 0.3807 \tag{42}$$

$$X_{of} = 1.6287 \tag{43}$$

X_{op} and X_{oz} are all needed to design the 3rd order Type PLL as in Figure 7. Assuming K_p is variable, its value can be calculated from (31) for a given ω_0. X_{of} for 3rd order is actually smaller than 2nd order, and what that means is, 3rd order will settle faster than 2nd order for the same ω_0. Let's check the phase margin for the 3rd order to ensure that it is stable. From (30), the phase margin can be calculated as follows,

$$PM = phase(1 + j\frac{\omega_o}{\omega_z}) - phase(1 + j\frac{\omega_o}{\omega_p})$$

$PM = 48.704°$

The phase margin for 3rd order is smaller than 2nd order. At PM of 48.704, the loop is still stable.

Part 2 of this article will appear in the next issue, continuing with a discussion of the 4th Order Type 2 PLL.

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